IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

Applicant: Sheehan D. Lake, et al.

Docket: BUR920020041US1 (16237)

Serial No.:

10/604296

Dated: June 18, 2003

Filed:

7-9-03

For: SYSTEM AND METHOD FOR DATA

PHASE REALIGNMENT

Commissioner for Patents P.O. Box 1450 Alexandria, VA 22313-1450

SUPPLEMENTAL INFORMATION DISCLOSURE STATEMENT

Sir:

In accordance with 37 C.F.R. §§ 1.97 and 1.98, it is requested that the following references, which are also listed on the attached Form PTO-1449, be made of record in the above-identified case.

1. DOSS AUS920010957, "Transferring data between domains having varying speed clocks";

CERTIFICATE OF MAILING UNDER 37 C.F.R. §1.8(a)

I hereby certify that this correspondence is being deposited with the United States Postal Service as first class mail in an envelope addressed to: Commissioner of Patents and Trademarks, P.O. Box 1450, Alexandria, VA 22313-1450 on 7-14-03.

Dated: 7-14-63

- 2. RD 434044, "Method to synchronize a low-frequency TAP clock to a high-frequency functional clock";
- 3. Japanese Patent No. JP 2001-265715 A, published August 16, 2001; and
- 4. Japanese Patent No. JP 8-55084, published October 25, 1995.

Applicant is submitting copies of the above-cited references.

Inasmuch as this Information Disclosure Statement is being submitted in accordance with the schedule set out in 37 C.F.R. § 1.97(b), no petition, certification or fee is required.

Respectfully submitted,

Steven Fischman

Registration No. 34,594

SCULLY, SCOTT, MURPHY & PRESSER 400 Garden City Plaza Garden City, New York 11530 (516) 742-4343

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EXAMINER: Initial if citation considered, whether or not citation is in conformance with MPEP Section 609; Draw line through citation if not in conformance and not considered. Include copy of this form with next communication to applicant.